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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,060	07/11/2003	Robert Jackson	15114H-068300US	4329

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,060	JACKSON, ROBERT	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelem (USP 5422833) who discloses a method/model/apparatus comprising:

(Claim 1)

defining respective functional representations (*functional representations (col 5 lines 11-19, col 6 line 64+), functional component (module) templates (col 9 line 27), functional component (module master) template (col 2 line 60+), functional elements, functional components and functional circuits in background, summary, col 7 lines 17-45, col 8 lines 6-19, claim 1)* of a plurality of system components (*system components = buses in abstract, background, summary, col 5, 7, claim 1*), each functional representation including at least one parameter value (*bus width in abstract, background, summary, col 7 line 17+, functional component widths (col 3 lines 8-9) or number of bits on bus (col 2 lines 20-22, col 3 line 56 to col 4 line 23, col 7 lines 1-53*); and

automatically defining an allowable set of such parameter values (*see abstract: "system propagates the data type and precision (precision =bus widths = parameter values) throughout the design automatically", see col 2 lines 16-17: "the width of the bus must be specified by the software"*) in dependence upon the plurality of system components (*bus widths, functional component widths (parameter values) for busses in dependence upon the plurality of system components (buses), i.e., bus widths depend on the number of bits and/or data lines and/or the number of conductors of/in busses (system components), i.e., col 2 lines 10-36, col 3 line 63+, col 7; also functional component widths depend on components),* the allowable set of parameter values defining compatible parameter values (see *"automatically to achieve circuit-wide consistency" and "bus width consistency" in abstract,* and *"bus widths must be consistent or at least compatible" in col 2 lines 22-23, and consistency of bus bits and precision (bus width) of bus in col 4 lines 18-25)*

(Claim 6)

a plurality of system components (*buses in abstract, background, summary, col 5, 7*), a model including a functional representation (*functional representations (col 5 lines 11-19, col 6 line 64+), functional component templates (col 9 line 27), module master template (col 2 line 60+), functional elements, functional components and functional circuits in background, summary, col 7 lines 17-45, col 8 lines 6-19, claim 1)* of the component concerned (*component concerned is on or more of: the bus or bus width selected/specified by designer (col 1 lines 61-63), "the width of the bus must be specified by the software" (col 2 lines 16-17), "bus widths must be consistent or at least compatible" (col 2 lines 22-23), "designer specifies the bus or functional component widths" and bus width, functional component width (col 3 lines 8-15)*) which representation includes at least one parameter value *(bus width in abstract, background, summary, col 1-2, col 7 line 17+, functional component widths (col 3 lines 8-9))* for the component.

(Claim 9)

a data storage medium (in *CAD system and computer in abstract, field of invention, background*) which is operable to store respective functional representations (*functional representations (col 5 lines 11-19, col 6 line 64+), functional component templates (col 9 line 27),module master template (col 2 line 60+), functional elements, functional components and functional circuits in background, summary, col 7 lines 17-45, col 8 lines 6-19, claim 1)* of a plurality of system components (*system components = buses in abstract, background, summary, col 5, 7, claim 1*), each functional representation including at least one parameter value (*bus width in abstract, background, summary, col 7, functional component widths (col 3 lines 8-9)*); and

a processor (in *CAD system and computer in abstract, field of invention, background*) which is operable to define automatically an allowable set of parameter values (*parameter values = precision =bus widths; see abstract: "system propagates the data type and precision (bus width) throughout the design automatically, see col 2 lines 16-17: "the width of the bus must be specified by the software"*), *also see bus widths* in *background, summary, col 7 line 17+)* for a selected group of system components

(one or more of: the bus or bus width selected/specified by designer (col 1 lines 61-63), "the width of the bus must be specified by the software" (col 2 lines 16-17), "bus widths must be consistent or at least compatible" (col 2 lines 22-23), functional component widths (col 3 lines 8-9))

(Claims 2, 10) wherein one of the system components is a bus (*see bus in abstract, background, summary, col 5, 7).*

(Claims 3, 8, 11) wherein the functional representation of the bus includes a parameter value *(number of bits on bus (col 2 lines 20-22, col 3 line 56 to col 4 line 23, col 7 lines 1-53))* relating to bus width.

(Claim 4) further comprising choosing an allowable set of parameter values (*select/specifying bus widths in col 1 line 61+, col 2 line16, data type and width col 3 lines 8-20 or number of bits on bus (col 2 lines 20-22, col 3 line 56 to col 4 line 23, col 7 lines 1-53))* and setting the parameter values of the functional representations concerned to the values defined by the chosen allowable set of parameter values.

(Claims 5, 13) selecting a plurality of system components *(select/specify busses in abstract, background, summary, col 7)*; selecting a connection for interconnecting (*lines/conductors in buses/components (col 2 lines 13-36, col 5 line10-12)*) such selected system components; and

selecting one of the allowable sets of parameter values (*buses or widths or functional component widths (col 3 lines 8-9) or number of bit on bus (col 2 lines 20-22, col 3 line 56 to col 4 line 23, col 7 lines 1-53)* in dependence upon said connection (*bus width and/or number of bits in a bus in dependence upon bus connection, i.e., depend on the number of bits and/or data lines and/or the number of conductors of/in busses (system components), i.e., col 2 lines 10-36, col 3 line 63+, col 7, also functional component widths depend on components)*)

(Claim 7) wherein the parameter relates to data transfer characteristics of the component (col 2 line 10, component = bus = for data transfer characteristics)

(Claim 12) wherein the processor is operable to choose an allowable set of parameter values *(bus widths in abstract, background, summary, col 7, functional component widths (col 3 lines 8-15) or number of bit on bus (col 2 lines 20-22, col 3 line 56 to col 4 line 23, col 7 lines 1-53)* and setting the parameter values of the functional representations concerned *to* the values defined by the chosen allowable set of parameter values (parameter values of the functional representations concerned *is one or more of: the bus or bus width selected/specified by designer (col 1 lines 61-63), "the width of the bus must be specified by the software" (col 2 lines 16-17), "bus widths must be consistent or at least compatible" (col 2 lines 22-23), "designer specifies the bus or functional component widths" and bus width,* template for each functional component (claim 1))

(Claims 14-15) a PLD *(fig 2, col 2 line 14, col 4 line 10, col 5 line 29+)*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner

Paul Dinh
11/5/04